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200mm N-Type SiC Substrate Specification

Parameter	Unit	Specification Value				Remark
Grade		Production Grade for MOS	Production Grade for SBD	Research Grade	Dummy Grade	
Diameter	mm	200±0.2		200±0.5		
Thickness	μm	350±25\500±25		350±40\500±40		
Polytype		4H-SiC				
Surface Orientation		4.0° toward<11 $\bar{2}$0>±0.5°			N/A	
Dopant		Nitrogen				
Resistivity	Ω·cm	0.017~0.028	0.015~0.028	0.01~0.030	N/A	
Notch Primary Flat rientation		<1 $\bar{1}$00>±1.0°		<1 $\bar{1}$00>±5.0°	N/A	
Notch	mm	1-1.5mm		0.5-2.0mm		
Secondary Flat Length		None				
LTV-Max	μm	≤2	≤3	≤4	≤5	10mm*10mm
TTV	μm	≤5	≤8	≤10	≤10	
BOW	μm	0±15	0±15	0±20	0±30	
Warp	μm	≤25	≤30	≤35	≤60	
Micropipe Density	cm-2	≤0.2	≤0.5	≤1	≤5	
TED	cm-2	<2000	<6000	<8000	<10000	KOH etching
BPD	cm-2	<600	<1000	<2000	<3000	KOH etching
TSD	cm-2	<200	<500	<1000	<3000	KOH etching
BSF/SF	% area	<1%		<5%	N/A	2m*2m grid

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Parameter	Unit	Specification Value				Remark
Grade		Production Grade for MOS1	Production Grade for SBD	Research Grade	Dummy Grade	
Metal Contamination	atoms/cm-2	<1E11		<1E12		K/Ca/Ti/V/Cr/Mn/Fe/Ni/Cu/Zn/A1/Na/
Back Scratch by highintensity light		None		N/A		By high-Intensity Light unaided eye
Surface Roughness	nm	C-face:mirror polished,Ra<3.0				AFM@5μm*5μm
		Si-face: CMP,Ra<0.2				
Foreign Polytypes*		None		Only allowed within 3mm edge exclusion area	Only allowed within 5mm edge exclusion area	
Polycrystal*		None		Only allowed within 3mm edge exclusion area	Only allowed within 5mm edge exclusion area	
Hex Plates by HighIntensity Light*		None		Only allowed within 3mm edge exclusion area	Only allowed within 5mm edge exclusion area	By high-intensity light unaided eye
Pinholes	number	None		1 allowed	N/A	
Cracks*	number	None		Only allowed within 3mm edge exclusion area	Only allowed within 3mm edge exclusion area	
EdgeChips	number	None		2 allowed,<1.0mm width & depth		
Scratch on Si face	mm	Cumulative scratch length <50	Cumulative scratch length <100	Cumulative scratch length <150	Cumulative scratch length <250	CS8520 or SiCA88
Stain (both faces)		None				

*Defects limits apply to entire wafer surface including the edge exclusion area.
Product with other specifications can be customized.

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